Inside ACA620EC – the economy accelerator

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Technical data

processor: Motorola MC68EC020-16, max. frequency 16.67MHz

ram: 16Mbyte SD-Ram 32-bit wide, 0-waitstate. Not usable in full.

logic/RAM frequency: 50MHz

CPU frequency: 50/3MHz (=16.67MHz in good approximation)

Programming the card

opening registers

The ACA620 has hidden registers located in 0xb8f000 and higher. After power-up, these registers are deactivated, so random read/write actions to these registers do not cause undesired operation. The following activation sequence is required to activate the ACA620 registers:

- write 0x8000 to 0xb8f000
- write 0x0000 to 0xb8f004
- write 0x8000 to 0xb8f008
- write 0x8000 to 0xb8f00c

after this procedure, the registers described in the next paragraph are available for reading/writing. A simple read from 0xb8f000 will deactivate the registers again. Activating and deactivating can be done at any time and any amount of times; there are no write-once registers.

Each register only uses bit 15 of the 16-bit word. The other bits are „don't care" on a write and contain no usable information on a read. The following description only refers to the usable bit of the registers. Only addresses on longword-offsets are used. The word-offsets in the middle between the used registers contain 0 in bit 15, so software can make a difference between the used bits (note that A1200 cards use a different bit!).

Identity registers: 0xb8f004 to 0xb8f014

Before you start poking any of the ACA registers, you should make sure that you're really talking to an ACA620. The following five bits should be checked:

- bit 15 of 0xbf8004 should be 1

- bit 15 of 0xbf8008 should be 0

- bit 15 of 0xbf800c should be 1

- bit 15 of 0xbf8010 should be 0

- bit 15 of 0xbf8014 should be 1

In addition to this ID, you can check for presence of autoconfig™ vendor 4626 (0x1212), product number 70 (0x46).

Maprom register: 0xb8f018

This bit is reset after a power-up and it is not altered on a normal reset. If this bit is set, the ROM spaces in 0xe0.0000 to 0xe7.ffff and 0xf8.0000 to 0xff.ffff are replaced with fast RAM, which appears like ROM. It is not writeable if the bit is set. The memory space can be filled while the maprom bit is reset: Writing to the ROM areas will „fall through" into RAM, but won't be readable until the maprom bit is set. CAUTION: The ROM space does not have any overlay-function. The computer will always see the true ROM vectors in 0x00.0000 after a reset, so any altered ROM should use the same addresses for vectors as the ones that the actually installed ROM chip uses. This is not true if the IRQovl bit is set (see further down).

Maxmem bit: 0xb8f034

This bit is reset after every system reset. While this bit is reset, the following address spaces are mapped to fastmem:

- 0x20.0000 to 0x5f.ffff (4M using autoconfig™)

- 0x60.0000 to 0x9f.ffff (4M)

- 0xc0.0000 to 0xcf.ffff (1M will be added by all Kickstart ROMs)

- 0xde.8000 to 0xde.ffff (32k as buffer mem and trampoline code area)

All other addresses will access the A600 mainboard, where the usual Amiga memory map applies. It is not recommended to add the 32k space at 0xde.8000 to the freemem list.

While this bit is set to 1, the following spaces are mapped to fastmem (in addition to the above spaces):

- 0xd0.0000 to 0xd7.ffff (512k)

- 0xa8.0000 to 0xb7.ffff (1M)

- 0xea.0000 to 0xf7.ffff (896k)

The Maxmem bit can be set and reset at any time. While reset, the contents of the unmapped memory areas stay unchanged and survive a system reset.

Expansion ROM protect bit: 0xb8f038

This bit is reset after a power-up and it stays unchanged on a reset. If set, the area from 0xf0.0000 to 0xf7.ffff will be write-protected. If the Maxmem bit is not set, this bit will re-map the second 4MByte block of fastmem (starting 0x40.0000) to the physical memory that is normally hidden by chipmem or IO/registers. See chapter "special memory mapping" on the next page.

IRQovl bit: 0xb8f03c

This bit is reset after power-up and it stays unchanged on a reset. It can be set and reset at any time. As a special function, this bit is always set automatically if an IRQ level 7 (NMI) is recognized. This auto-set function on IRQ7 cannot be disabled, so proper preparation must be performed before the first IRQ7 is triggered.

The IRQovl bit affects mapping of the first 4k in address space (addresses 0x00.0000 to 0x00.0fff) and the second megabyte of chipmem space (addresses 0x10.0000 to 0x1f.ffff). When reset, these areas contain chipmem, and fastmem contents are not changed on a write. When set, this area is mapped to fastmem, and chipmem is not changed on a write. Since most Kickstart versions use the lowest chipmem area for copperlist and other chip register access, it is not practical to leave this bit on during normal operation of the computer. Instead, it should only be used as a trampoline area for the case where a Level7 IRQ is triggered. While in a special "freezer monitor" mode, the extra 1M of fastmem at 0x10.0000 can be used for backing up chipmem contents of the lower 1M chipram. You can then open a screen and use 1020k chipmem for the monitor without losing any memory contents – neither fastmem nor chipmem, even if full memory of the card is used.

For further buffering and checking the "hidden" chipmem in this "freezer/monitor" mode, please consider using the 0xde.8000 area, which is always available (independent of any bit settings) and can be used for peeking and altering the hidden chipmem areas. Also, this 32k area can be used to restart the interrupted program without altering the contents of any other memory area.

Special memory mapping

If the Maxmem bit is reset, but the expansion ROM protect bit is set, the memory area from 0x40.0000 to 0x7f.ffff will contain the memory areas that would normally be unavailable due to IO and chipmem areas covering this memory. In order to make almost all physical memory available to special software, this bit setting will move:

0x00.0000-0x0f.ffff to 0x40.0000-0x4f.ffff

This Fastram area is normally covered by the lower 1MByte of chipmem. Caution: This includes lowest 4k that is used by the IRQovl function. Make sure that your software does not accidentally overwrite this memory area, as it contains all CPU vectors in case that VBR is 0.

0xd0.0000-0xdf.ffff to 0x50.0000-0x5f.ffff

The lower half of this area is available with the Maxmem option, and the upper half from 0xd8.0000 and higher is normally covered by IDE, RTC and chip registers. Caution: This

also includes the 32k area from 0xde.8000 that is always visible. Make sure that your software does not accidentally overwrite this memory area, as it might be used as a jump-target for Level-7 IRQs.

0xa0.0000-0xaf.ffff to 0x60.0000-0x6f.ffff

The upper half of this fastmem area is available with the Maxmem option, and the lower half is normally covered by PCMCIA/Gayle registers.

0xb0.0000-0xbf.ffff to 0x70.0000-0x7f.ffff

The lower half of this fastmem area is available with the Maxmem option, and the upper half is normally covered by CIA registers and the ACA620 registers.

Alltogether, this option lets you use the hidden 2.5MByte of the physical memory, for example for a reset-proof RAM disk.

Overclocking

Simulation of the CPLD and memory show that the maximum system clock is 50.7MHz. The oscillator should therefore not be exchanged for anything faster. The CPU's maximum frequency of 16.67MHz (given in the data book) is exactly met with the timing configuration that the accelerator has been shipped with. It is therefore not recommended to decrease the clock divider to 2, because the CPU cannot be guaranteed to run stable at 25MHz. At 16.67MHz, the CPU already produces considerable heat that is barely dissipated through the ventilation hole on the CPU card. At higher speeds, memory timing will be met, but a heat sink for the CPU will be required.

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